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Family of a novel 3 bit Flash ADC

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Abstract: Analog –to-digital converter is an important device has a huge application in todays digitized world. Flash converter is high speed converter among all other ADCs. It consists of 2^N comparators that provide thermometer coded ouput which is converted to a digital output by an encoder. In high speed ADCs comparator plays an important role for high speed application using minimization techniques. The main disadvantage of flash type ADC is power hungry so the aim is to design low power flash type ADC with low power comparator. The design issues are related to gain, phase, gain bandwidth, resolution, speed, area and power dissipation. Simple two stage opamp with miller capacitance can be used as a high gain comparator. It can be easily operated at low power. It is simulated in 180nm technology using cadence virtuoso analog design environment simulation. The op-amp uses a 1.8volt Vdd and a -1.8volt Vss and consumes a power of around 0.9mW (as per post layout simulations). The analog output of each comparator is encoded using cascading full adder designed by pass transistor logic that makes the circuit more faster.

Keywords: string of pmos load, Two stage amplifier, miller capacitance, full adders.

I. INTRODUCTION

In last few years the largest portion of electronics industry is dominated by MOS market. It becomes a challenging to design analog circuit reducing its feature sizes, supply voltages as well as transistor channel length.

Op amp can easily trade-off between all performance parameters like gain, phase, phase margin, unity gain bandwidth etc. The design can be achieved handling various aspect ratios i.e changing width and length of transistors to be in saturation region so that it can give better performance. This paper, is discussed on flash-type ADC and a novel design involves a new approach towards the OP-AMP and the encoder.

Traditionally, a flash-type ADC involves different components to design: comparators, resistors, logic gates. This paper introduces a low-power OP-AMP modified from the traditional one, and an encoder employing cascaded full adders with pass transistor logic gates.

II. BASIC BUILDING BLOCKS

Figure 1. shows the basic circuit diagram of a 3 bit Flash ADC. Flash type ADC employs with 2^{N-1} number of comparators, 2^N resistors and encoder for N bit resolution. An analog input is fed to each voltage comparator to compare input voltage to successive reference voltages.

Reference voltage ladder is constructed with resistive ladder but to reduce the chip area complexity a series of pmos load is used as reference voltage ladder. To reach at VDD R1 & R8 is taken as 2 Kohm whether others are 1Kohm.

Each comparator produces 1 when Vref is less than Vin otherwise it produces 0. The compared analog input is fed to the binary encoder to get digitized output.

These are the basic building block of a flash ADC.

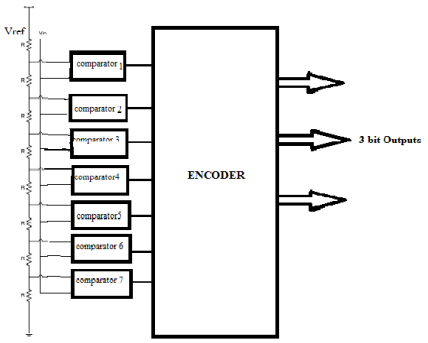

Fig 1: Circuit diagram of a 3bit Flash type ADC

III. DESIGN PROCEDURE

Comparator is the main feature of ADC design. Common two staged opamp is used in comparator design that can be extensively used in ADC applications. Figure 2 shows basic structure of a two- stage CMOS opamp has two operational stages.

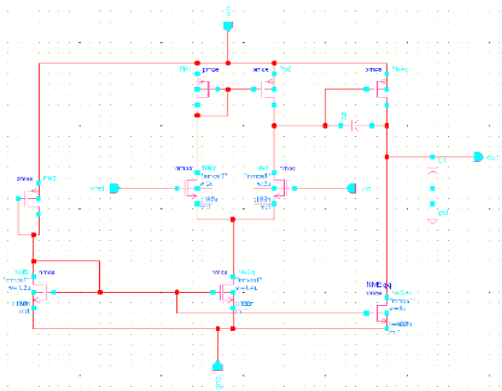

Fig 2: Circuit diagram of a basic two stage opamp[1]

- First stage consists of differential amplifier as input amplifier which is used for high noise immune.
- Second stage consists of common source amplifier as output amplifier used for high gain.

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A current mirror is used as a biasing circuit that is free from voltage sources and utilize current as a reference source.

A miller compensation capacitor is used to maintain the stability of the circuit and increase phase margin.

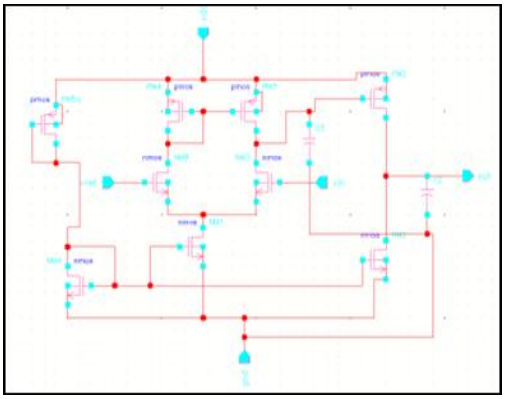

Fig 3: Schematic design of Comparator

The length and width of transistors are scaled down to assume transistors are in saturation for actual result. So proper sizing is essential to get proper gain and phase. Table I shows the scaling effects of various transistors.

Table I Effect of parameter after scaling

Increase of Parameters	Drain Current I_5	M1 & M2 W/L L	M3 & M4 L	M6 W/L	M7 L	C_c
DC gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$ $\uparrow$	$\uparrow$	$(\uparrow)^{1/2}$	$\uparrow$	
Phase	$\downarrow$	$\uparrow$		$\downarrow$	$\downarrow$	
GB	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$				$\downarrow$
SR	$\uparrow$					$\downarrow$

Two stage opamp is modified in the proposed design shown in Fig.3 is to improve the performance parameter of the comparator circuit. The compensation capacitor is grounded and proper sizing is done by minimizing length of various transistors according to the performance of the circuit.

Table II Specifications of Comparators

Specifications	Basic Comparator	Proposed Comparator
Technology	180-nm	180-nm
Power supply	1.8 V	1.8 V
Input Voltage Range	0 to 1.8 V	0 to 1.8 V
Frequency	100MHz	100MHz
Cc	2.2pF	0.2pF
C_L	10pF	5pF
UGB	15.415 MHz	52.04 MHz
Gain	66.7dB	68dB
Total Power dissipation	145.324µW	144.0633 µW

The architecture of the schematic is designed by cadence tools in 180 nm technology.

IV. ENCODER

Encoder is a digital circuit that converts an active input signal into a coded output signal. Consider encoder has n input lines and only one of which is active at any time and m output lines. It encodes one of the active inputs to a coded binary output with m bits.

In this paper encoder circuit is designed using cascading 10 transistors full adders to reduce complexity of the circuitry. Fig 4 shows the circuit diagram of 10T full adder using XOR and XNOR logic gates.

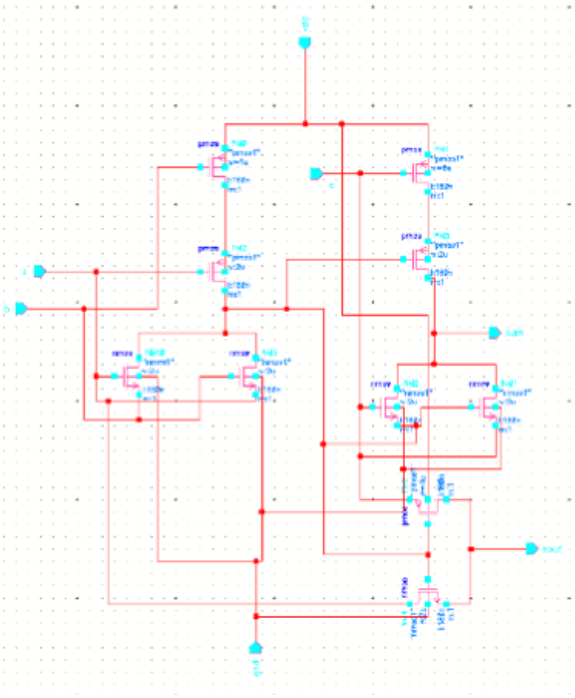

Fig 4: 10T Full adder circuit

This full adder is utilized in ADC circuit as an encoder. The chip complexity, area is reduced in this design. Fig 5 shows the cascaded encoder circuit using pass transistor logic.

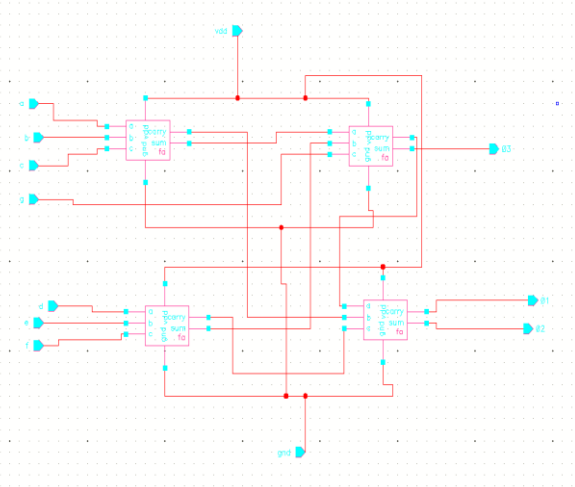

Fig 5: encoder circuit

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Table III TRUTH TABLE FOR THERMOMETER TO BINARY ENCODER[2]

THERMOMETER CODE							OUTPUT BINARY CODE		
O7	O6	O5	O4	O3	O2	O1	B3	B2	B1
1	1	1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1	1	0
0	0	1	1	1	1	1	1	0	1
0	0	0	1	1	1	1	1	0	0
0	0	0	0	1	1	1	0	1	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0	0

V. FLASH ADC

Fig 6 shows the custom design of ADC providing its all components together.

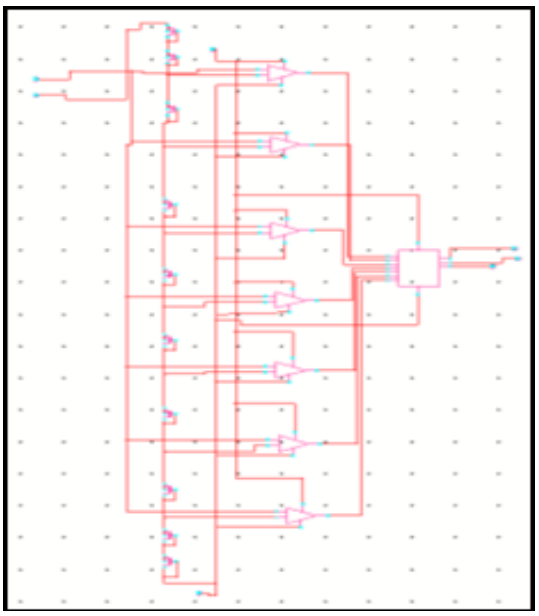

Fig 6: Circuit diagram of FADC

VI. RESULTS & DISCUSSION

The designed schematic is simulated in virtuoso platform of cadence. A sinusoidal input signal is applied to the non-inverting terminal of the comparator and a reference dc voltage to the other input. It gives following waveform for the comparator output.

a. Output waveform of Comparator

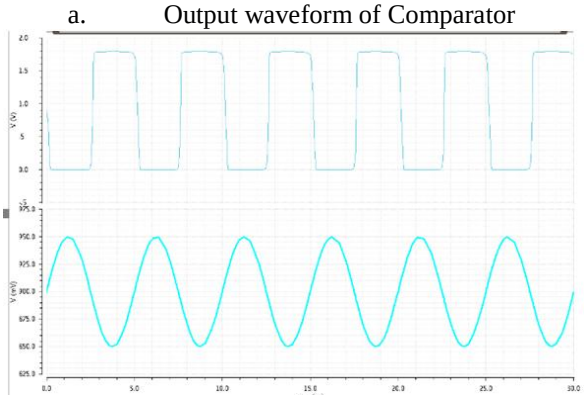

Fig 7: Comparator output

AC analysis is performed to get DC gain of 68dB, phase and UGB is 52.04 MHz of the comparator circuit.

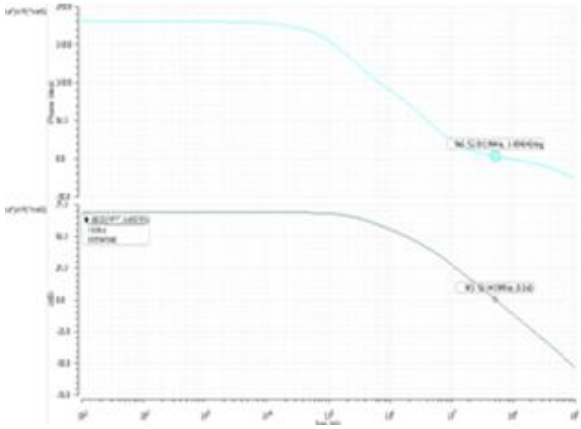

Fig 8: AC Analysis of Comparator

b. Output waveform of Encoder:

Fig 9 shows the waveform of encoder circuit is obtained by transient analysis where stop time is 100ns.

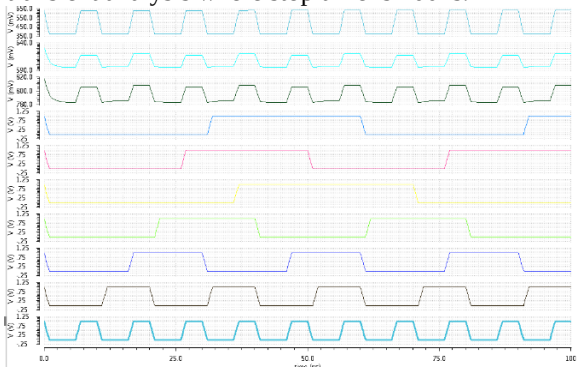

Fig 9: Encoder output

c. Output waveform of Flash ADC

The input signal is applied as sine wave to implement and simulate transient analysis of 3 bit Flash ADC in 180nm technology using Virtuoso analog environment design of cadence tools.

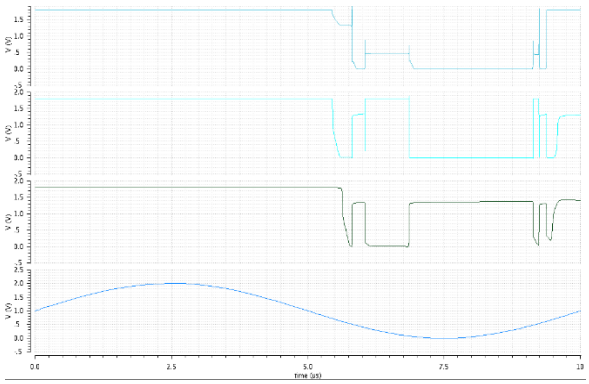

Fig :10 Flash ADC output

VII. CONCLUSION

This paper concludes the full custom design of a two stage CMOS Op-Amp and analysis of its behaviour with various aspect ratios using minimizing techniques. The obtained results show that the designed amplifier has successfully satisfied all the specifications given in advance. Tables

and graphs of different parameters are drawn. Though Flash ADC is power hungry and complex circuit, so it is a challenge to design and implement low power ADC with high speed applications. Moreover, this architecture can be extended the medium-to-high resolution applications because of the circuit simplicity [2].

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BIOGRAPHY

Sarojini Mandal recieved B.Tech Degree from Future Institute of Engineering & Mangament Kolkata. Received M.tech Degree from KIIT University Bhubaneswar Odisha. Area of interest is VLSI Design and Embedded System.

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